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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,432	04/30/2001	Aaron W. Buchwald	1875.0560001	9072

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EXAMINER	
PERILLA, JASON M	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,432	BUCHWALD ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5-9/01 6-7/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statements (IDS) are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: ***fig. 10, ref. 1000 and fig. 9, refs. 910a-d***. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. It is requested by the Examiner that the Applicant make the appropriate amendments to the specification to correct the known minor clerical and typographical errors present in the specification. The Applicant is directed to the

Patented US Application No. 09/844266 (Attorney Docket # 1875.0560005) having an identical specification wherein corrections have been made.

Claim Objections

5. Claims 6-10, 12, 18, and 20 are objected to because they relate to frequency offsets or frequency errors. The instant application is related to the correction of a phase difference between a data signal and the sampling signal used to sample the data signal. However, where the claims include limitations relating to a frequency error or a frequency offset, it is suggested by the Examiner that the claims are amended to use limitations of phase error or phase offset because the use of the term phase more closely embodies the true meaning of the invention. Where one skilled in the art is familiar with the relationship between phase and frequency, the use of "frequency offset" may cause one to misinterpret the claims to be relating to a system or method of automatic frequency correction or control. The estimation of a frequency offset in a system for correcting phase may make the claims indefinite because it becomes unclear if the system corrects phase differences or frequency differences.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-11 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1-3, the specification does not enable one skilled in the art to "rotate the interpolated phase of the sampling signal **at a rate corresponding to the frequency offset**". The specification is related to the phase alignment of a data signal with a sampling signal. The specification does not relate to or enable one skilled in the art to modify any frequencies. Further, the rotation of the interpolated phase output signal does not occur according to the "rate of the frequency offset" as claimed. The rate at which the interpolated output is *adjusted or updated* is most clearly understood to be at the rate of the sampling frequency according to the drawings. However, the specification does not enable one to adjust or update the interpolated output according to the *rate of the* ***frequency offset***.

Regarding claim 4, the specification does not enable one skilled in the art to decrease or increase the frequency of the interpolated sampling signal. Rather, the specification describes the phase advance or phase retard of the interpolated output signal. The terms frequency and phase can not be used interchangeably in such a claim limitation. Indeed, it is the phase, not the frequency, that is adjusted by the phase interpolator, and one skilled in the art is not enabled otherwise according to the specification.

Claims 5-11 are rejected as being based upon a rejected parent claim.

Regarding claim 15, the specification does not enable one skilled in the art to decrease or increase the frequency of the interpolated sampling signal. Rather, the specification describes the phase advance or phase retard of the interpolated output signal. The terms frequency and phase can not be used interchangeably in such a claim limitation. Indeed, it is the phase, not the frequency, that is adjusted by the phase interpolator, and one skilled in the art is not enabled otherwise according to the specification.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Evans et al (US 6002279 – IDS paper no. 6 ref. AE1; hereafter "Evans").

Regarding claim 1, Evans discloses by figure 3 a system for recovering timing information from a serial data signal (abstract), comprising: a phase interpolator (304; col. 4, lines 23-26) adapted to derive a sampling signal having an interpolated phase in response to a plurality of control signals (output from VCO 302; col. 4, lines 18-23); and a controller (306) including a data path ("DATA" in path) adapted to sample the serial data signal according to the sampling signal (fig. 7C; "RECOVERED DATA"), a phase detector (fig. 7B) adapted to detect a phase offset between the sampling signal and the serial data signal (col. 5, lines 3-16), a phase error processor (308) coupled to the phase detector and adapted to estimate a frequency offset between the sampling signal

and the serial data signal based on the phase offset (fig. 8B; col. 5, lines 27-38), a command generator (fig. 3, ref. 310; fig. 9; col. 5, line 59-col. 6, line 36) coupled to the phase error processor and adapted to generate a rotator control signal in response to the frequency offset estimate, and a control signal rotator adapted to manipulate the control signals (fig. 5, refs. 502, 504, 506, and 508) in response to the rotator control signal, whereby the controller causes the phase interpolator to rotate the interpolated phase of the sampling signal at a rate corresponding to the frequency offset. Reference 306 of figure 3 "UP/DOWN DETECT" of Evans is both a sampler (fig. 7C) because it recovers the digital data as well as a phase detector (fig. 7B) because it detects a lead or lag relationship between the input signal and the recovered clock signal. The controller divides the UP/DOWN signals from the phase detector by the phase error processor (308) to estimate a frequency offset between the sampling signal and the serial data signal. The output of the phase error processor is input to the command generator (fig. 3, ref. 310; fig. 9) which is adapted to rotate the plurality of phase control signals and correspondingly the interpolated phase of the timing signal so as to reduce the phase offset between the timing signal and the serial data signal (col. 5, lines 5-16; fig. 10, col. 6, lines 29-35).

Regarding claim 2, Evans discloses by figure 3 a system for recovering timing information from a serial data signal (abstract), comprising: a phase interpolator (304) adapted to derive a sampling signal having an interpolated phase; and a controller (refs. 306, 308, and 310) coupled to the phase interpolator and including a phase error processor (308) adapted to derive an

estimate of a frequency offset between the sampling signal and the serial data signal, the controller being adapted to cause the phase interpolator to rotate the interpolated phase of the sampling signal at a rate corresponding to the frequency offset so as to reduce the frequency offset between the sampling signal and the serial data signal (col. 5, lines 5-16; fig. 10, col. 6, lines 29-35).

Regarding claim 3, Evans discloses the limitations of claim 2 as applied above. Further Evans discloses that the controller causes the phase interpolator to repetitively rotate the interpolated phase of the sampling signal through a range of phases spanning 360 degrees (fig. 10; col. 4, lines 40-60) at the rate corresponding to the frequency offset (col. 6, lines 1-11).

Regarding claim 4, Evans discloses the limitations of claim 2 as applied above. Further Evans discloses (col. 5, lines 5-16) that the controller includes logic adapted to cause the phase interpolator to: rotate the interpolated phase of the sampling signal in a direction of increasing phase to decrease a frequency of the sampling signal when the frequency offset estimate indicates a frequency of the sampling signal is greater than a frequency of the serial data signal (D1=D2<>D3); and rotate the interpolated phase of the sampling signal in a direction of decreasing phase to increase the frequency of the sampling signal when the frequency offset estimate indicates the frequency of the sampling signal is less than a frequency of the serial data signal (D1<>D2=D3). Evans discloses (col. 5, lines 5-16) that the rotator control signal is one of a phase-advance (D1=D2<>D3), a phase-retard (D1<>D2=D3), and a phase-hold signal (D1=D2=D3), the phase control signal rotator being adapted to: rotate the

plurality of phase controls signals in a first direction to advance the interpolated phase of the timing signal in response to the phase-advance signal (col. 5, line 63 – col. 6, line 2); rotate the plurality of phase controls signals in a second direction to retard the interpolated phase in response to the phase-retard signal (col. 6, lines 2-3); and prevent the plurality of phase control signals and correspondingly the interpolated phase from rotating in response to the phase-hold signal (col. 6, lines 4-6).

Regarding claim 5, Evans discloses the limitations of claim 2 as applied above. Further, Evans discloses that the phase interpolator includes: a plurality of reference stages (fig. 5, refs. 502, 504, 506, and 508) adapted to control individual magnitudes of a plurality of component signals having different phases responsive to the plurality of phase control signals (col. 4, lines 30-40); and a combining node (fig. 5, ref. 510) adapted to combine the plurality of component signals into the interpolated timing signal.

Regarding claim 6, Evans discloses the limitations of claim 2 as applied above. Further, Evans discloses that the controller includes: a data path ("DATA" in path) adapted to sample the serial data signal according to the sampling signal (fig. 7C; "RECOVERED DATA"), thereby producing serial data samples; a phase detector (fig. 7B) coupled to the phase error processor and adapted to detect a phase offset between the sampling signal and the serial data signal based on the serial data signal, the phase error processor (fig. 3, ref. 308) being adapted to estimate the frequency offset between the sampling signal and the serial data signal based on the phase offset.

Regarding claim 7, Evans discloses the limitations of claim 2 as applied above. Further, Evans discloses that the controller includes a phase detector (fig. 3, ref. 306; fig. 7B) adapted to detect a phase offset between the sampling signal and the serial data signal (col. 5, lines 3-15), the phase error processor being adapted to estimate the frequency offset between the sampling signal and the serial data signal based on the phase offset (col. 5, lines 39-46).

Regarding claim 8, Evans discloses the limitations of claim 2 as applied above. Further Evans discloses that the controller is adapted to apply a plurality of phase control signals to the phase interpolator to control the interpolated phase of the sampling signal, the controller being adapted to manipulate the plurality of phase control signals, and correspondingly, the interpolated phase of the sampling signal, based on the frequency offset estimate (fig. 5; fig. 10).

Regarding claim 9, Evans discloses the limitations of claim 2 as applied above. Further Evans discloses that the controller is adapted to rotate the plurality of phase control signals, and correspondingly, the interpolated phase of the sampling signal according to the frequency offset estimate (abstract).

Regarding claim 10, Evans discloses the limitations of claim 2 as applied above. Further Evans discloses by figure 3 that the controller further includes: a command generator (310) coupled to the phase error processor (308) and adapted to generate a rotator control signal in response to the frequency offset estimate; and a control signal rotator (fig. 5, refs. 502, 504, 506, and 508) adapted to apply a plurality of phase control signals (fig. 5, "4 PHASES FROM VCO") to the phase interpolator to control the interpolated phase of the sampling

signal, the control signal rotator being adapted to rotate the plurality of phase control signals, and correspondingly the interpolated phase (fig. 5, "PHASE INTERPOLATED OUTPUT") of the sampling signal, at the rate corresponding to the frequency offset, responsive to the rotator control signal. In figure 5, the rotator control signals from the command generator (310) are shown as "DAC CONTROL LINES" and the interpolated phase output is responsive to the control signal rotators having the rotator control signals as inputs.

Regarding claim 11, Evans discloses the limitations of claim 10 as applied above. Further Evans discloses (col. 5, lines 5-16) that the rotator control signal is one of a phase-advance (D1=D2<>D3), a phase-retard (D1<>D2=D3), and a phase-hold signal (D1=D2=D3), and step (c) comprises: rotating the plurality of phase controls signals in a first direction to advance the interpolated phase of the timing signal in response to the phase-advance signal (col. 5, line 63 – col. 6, line 2); rotate the plurality of phase controls signals in a second direction to retard the interpolated phase in response to the phase-retard signal (col. 6, lines 2-3); and prevent the plurality of phase control signals and correspondingly the interpolated phase from rotating in response to the phase-hold signal (col. 6, lines 4-6).

Regarding claim 12, Evans discloses by figure 1 a method of recovering timing information from a serial data signal (abstract), comprising: (a) deriving a sampling signal having an interpolated phase (304; col. 4, lines 22-25); (b) estimating a frequency offset between the sampling signal and the serial data signal (col. 5, line 59 – col. 6, line 13); and (c) rotating the interpolated phase of the sampling signal at a rate corresponding to the frequency offset, thereby

reducing the frequency offset between the sampling signal and the serial data signal (fig. 10, col. 6, lines 29-35).

Regarding claim 13, Evans discloses the limitations of claim 12 as applied above. Further Evans discloses that step (b) comprises: detecting a phase offset between the serial data signal and the sampling signal (fig. 7B; col. 5, lines 3-15); and estimating the frequency offset based on the phase offset (abstract; col. 5, lines 47-58).

Regarding claim 14, Evans discloses the limitations of claim 12 as applied above. Further Evans discloses that step (c) comprises repetitively rotating the interpolated phase of the sampling signal through a range of phases spanning 360 degrees (fig. 10; col. 4, lines 40-60) at the rate corresponding to the frequency offset (col. 6, lines 1-11).

Regarding claim 15, Evans discloses the limitations of claim 14 as applied above. Evans further discloses that step (c) further comprises: rotating the interpolated phase of the sampling signal in a direction of increasing phase (UP) to decrease a frequency of the sampling signal when the frequency of the sampling signal is greater than a frequency of the serial data signal; and rotating the interpolated phase of the sampling signal in a direction of decreasing phase (DOWN) to increase the frequency of the sampling signal when the frequency of the sampling signal is less than the frequency of the serial data signal (col. 5, lines 3-15). The rejection of claim 4 above follows that of instant claim 15.

Regarding claim 16, Evans discloses the limitations of claim 12 as applied above. Evans further discloses that step (a) comprises deriving the sampling

signal phase responsive to a plurality of phase control signals (fig. 5, "4 PHASES FROM VCO; col. 4, lines 15-23), the method further comprising manipulating the plurality of phase control signals responsive to the phase offset.

Regarding claim 17, Evans discloses the limitations of claim 16 as applied above. Evans further discloses that step (a) comprises deriving the (interpolated) sampling signal phase responsive to a plurality of phase control signals (fig. 5, "DAC CONTROL LINES"); and step (c) comprises rotating the plurality of phase control signals (fig. 10), and correspondingly, the interpolated phase of the sampling signal according to the phase offset. The interpolated phase of the sampling signal is rotated according to the plurality of phase control signals which are generated according to the phase offset between the received data and the interpolated signal.

Regarding claim 18, Evans discloses the limitations of claim 12 as applied above. Evans further discloses that step (b) comprises: sampling the serial data signal according to the sampling signal (fig. 7C; col 5, lines 17-27), thereby producing serial data signal samples ("RECOVERED DATA"); deriving a frequency error signal (col. 5, lines 3-15) indicative of the frequency offset between the timing signal and the serial data signal based on the serial data signal samples.

Regarding claim 19, Evans discloses the limitations of claim 12 as applied above. Evans further discloses that step (a) comprises: controlling individual magnitudes of a plurality of component signals having different phases responsive to a plurality of phase control signals (fig. 5, col. 4, lines 30-40); and

combining the plurality of component signals into the sampling signal having the interpolated phase (fig. 5, ref. 510).

Regarding claim 20, Evans discloses the limitations of claim 12 as applied above. Evans further discloses that step (c) comprises synchronizing a frequency of the sampling signal to a frequency of the serial data signal (abstract). The purpose of the phase interpolator of Evans is to phase or frequency synchronize the sampling signal frequency to the frequency of the serial data signal.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art not relied upon above is cited to further show the state of the art with respect to phase interpolators.

U.S. Pat. No. 5945862 to Donnelly et al.

U.S. Pat. No. 5703905 to Langberg.

U.S. Pat. No. 5554945 to Lee et al.

U.S. Pat. No. 5614855 to Lee et al

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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July 1, 2004

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